Siddhesh Eknath Shinde

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SUMMARY

Computer Engineering graduate student with experience in RTL design, microarchitecture, and SystemVerilog, seeking an RTL Design internship focused on AI hardware.

EDUCATION

North Carolina State University **Raleigh, NC**

Master of Science in Computer Engineering; GPA:3.0/4.0 *August 2025 - May 2027*

Relevant Courses: Embedded Systems Architecture, Architecture of Parallel Computers, Neural Network and deep learning, ASIC Verification, Microprocessor Architecture, ASIC and FPGA Design with Verilog.

Pune University **Pune, India**

Bachelor of Engineering in Electronics and Telecommunication; GPA: 3.6/4.0 *August 2021 - June 2025*

Relevant Courses: VLSI design, Digital Circuits, Analog Circuits, Electrical/Electronic Circuits, Control Systems, Power Electronics.

TECHNICAL SKILLS

Languages: C, C++, Verilog, System Verilog (SVA), Python, Bash, TCL, RISC-V Assembly.

RTL / Design: RTL Design, Microarchitecture, SoC Design, Subsystem Design, Design for Synthesis, Performance/Area/Power Optimization, Low-Power Design, Digital Logic Design, Timing-Aware RTL Design

Tools: Questa/ModelSim, VCS, GDB, Linux, Unix, Git, Synopsys, Cadence.

Relevant Areas: Computer Architecture, Pipelined Processor Design, High-Performance Digital Design, SoC Integration, Waveform Debug, Timing and Power Analysis.

PROJECTS

Intel Processor Testbench Implementation (Google/Skywater 130nm Open PDK) *August 2025 – December 2025*

- Executed a complete RTL-to-GDSII physical design flow using Synopsys ICC2, achieving a 43% improvement in composite PPAT metric through clock-tree synthesis and place-and-route with zero timing violations.
- Investigated PPAT tradeoffs and developed a TCl-based implementation methodology to enforce DFM-aware routing constraints, achieving full static timing closure with an 8.24 ns critical path delay.

FIR Filter Accelerator for RISC-V SoC *August 2025 – December 2025*

- Developed a 16-tap FIR accelerator IP with 64-bit packed I/O and DMA integration, achieving ~30.6× performance improvement over software baseline with zero computational error.
- Implemented a compact ~49K-unit design using fully unrolled parallel MACs and register-based storage, with II=2 pipelining at a 1.396 ns critical path.

I2C Multi-Bus Controller (I2CMB) Design Verification and Coverage Closure *January 2026 - ongoing*

- Developed a layered SystemVerilog SoC-style verification environment for a Wishbone-controlled I2CMB with scoreboard-based checking, directed/random tests, and coverage collection in Questa/ModelSim.
- Authored a 20-item coverage-driven verification plan and achieved 84.66% coverage closure across register, transfer, and FSM scenarios through regression debug and analysis.

DRAM-Streamed CNN Accelerator in SystemVerilog (4X4 Conv + LeakyReLU + 2X2 AvgPool) *August 2025 – December 2025*

- Designed a high-throughput SystemVerilog CNN accelerator implementing 4x4 convolution, LeakyReLU, and 2x2 average pooling for streamed image processing workloads.
- Built and validated memory-efficient dataflow logic using sliding-window and ping-pong buffering techniques to sustain continuous operation and reduce redundant DRAM access.

Out-of-Order Superscalar Pipeline Simulator (Dynamic Instruction Scheduling – RISC V) *August 2025 – December 2025*

- Built a cycle-accurate superscalar core simulator to analyze IPC sensitivity, backend bottlenecks, and microarchitectural tradeoffs across workloads.
- Implemented realistic backend timing (dependency tracking, wakeup/ready, oldest-ready issue with sequence numbers, pipelined int/mul/mem latencies) and generated/validated cycle-accurate per-instruction stage timelines.

Computer Architecture Simulator Suite (Branch Prediction and Cache Analysis) *August 2025 – December 2025*

- Built C/C++ simulators for branch prediction and configurable L1/L2 cache hierarchies, implementing bimodal, gshare, and hybrid predictors along with set-associative caches, LRU replacement, WBWA policy, and stream-buffer prefetching.
- Improved prediction accuracy by up to 18% on SPEC benchmarks and increased cache hit rate by 15–20%.

WORK EXPERIENCE

TDL TechSphere — Project Intern | RFID based attendance system using PCB *August 2024 – May 2025*

- Designed, integrated, and debugged an RFID-based attendance system on a custom PCB using a microcontroller, RFID reader, LCD, and GSM module for real-time identification and notification.
- Performed board bring-up, prototype validation, and PCB debugging of the 5V power subsystem using an oscilloscope and DMM, resolving voltage stability and ripple issues.